LOW INDUCTANCE PARALLEL PLATE INTERCONNECTIONS FOR POWER SEMICONDUCTOR SWITCHES

This report addresses the issues around the necessity to frequently operate with a high rate of change of current in power semi-conductor circuits – particularly stray inductance. It refers to, and provides examples of, a solution of using parallel conducting plates.

It concludes that the use of parallel conduction plates separated by insulation to form the 'go' and 'return' paths for interconnections has successfully reduced the circuit stray inductance by a factor greater than 10. Without this method of interconnection, the power semiconductor switch (a transistor in the present case) would have to be considerably de-rated. The main disadvantages are that the design costs are moderate to high and must include allowances to achieve component terminal and mounting tolerances of about 0.5mm. Modification may be awkward.

For production equipment, even in small quantities, parallel plate connections offer much lower production, as compared with conventional cable costs.

Insulation may be moulded to reduce costs, and thin conductive sheets, particularly for low powers may be produced using P.C.B technology.

As power switching semiconductors reach higher speeds and powers, it is likely that parallel plate interconnections will be adopted to an increasing extent.

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